

# Good OMENs

## Purdue researchers match experimental results with simulations of nanoscale transistors using Ranger

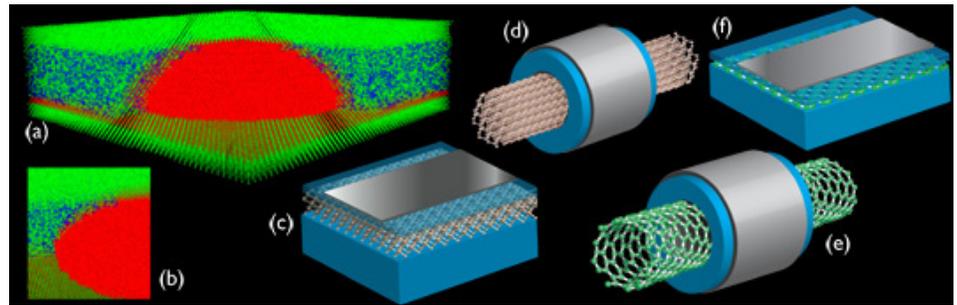
After more than 12 years of research and development, simulation tools that represent the electrical and material characteristics of nanoscale transistors are now robust enough to guide experiments.

Drs. Mathieu Luisier and Gerhard Klimeck, researchers at Purdue University’s Network for Computational Nanotechnology, built the OMEN simulation framework to model the movements of electrons through nanoscale semiconductor devices in 3D. Their system enables researchers to better predict the behavior of experimental transistor designs, including those made of silicon, as well as less conventional materials.

In 2009, Luisier and Klimeck proved the efficacy of their technique by matching the physical lab results of Jesus A. del Alamo, a professor at the Massachusetts Institute of Technology (MIT), for a novel high electron mobility transistor (HEMT) that uses indium-arsenide as its channel material.

“We reproduced their experimental data in both the ON and OFF states of the device,” said Luisier. “This could be achieved by properly accounting for the tunneling currents flowing through the insulator layers of the devices. As far as I know, there is no other device modeling tool capable of such a physical accuracy and scaling as OMEN.”

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Nanoelectronic device geometries. (a) The multimillion-atom Nanoelectronic Modeling 3D (NEMO-3D) simulation geometry of an Indium arsenide (InAs) quantum dot on a Gallium arsenide (GaAs) substrate, capped by an alloy Indium aluminum arsenide (InAlAs) strain-reduction layer. (As atoms were omitted for clarity’s sake.) (b) A zoom view of (a) from a different angle. Among the several 2D and 3D device geometries for OMEN transport simulations are (c) an ultra-scaled thin body transistor, (d) a gate-all-around nanowire, (e) a gate-all-around carbon nanotube, and (f) a top-gated graphene sheet.

The difficulties in simulating nano-scale transistors are due in large part to the problems involved in building and operating devices only a few nanometers in width. As devices shrink beyond a certain size threshold, quantum mechanical effects are revealed, causing transistors to exhibit different behavior. Strange phenomenon like quantum tunneling and phonon scattering diminish the efficiency of the device or make it heat up beyond acceptable limits. The functional importance of these quantum effects means they need to be included in the simulation code, which entails solving the Schrödinger wave equation repeatedly, a computationally intensive task.

These nanoscale, quantum characteristics have slowed chip development and now threaten to derail “Moore’s Law,” which predicts that the number of transistors that can be placed on an integrated circuit will double every two years. In fact, CPU speeds have increased little in the last few years, in part because of these quantum-level complexities.

“A lot of heat is being generated in these transistors as they switch on and off,” Klimeck said. “We’re asking ourselves: can we consume less power in a device and allow the electrons to move faster through the structure?”

“Mobility” measures the velocity of electrons as they move through a material. Silicon has low mobility; this limits the speed of calculations as electrons struggle to pass through tiny gates. Alternative semi-conducting materials, like indium-arsenide and graphene (another system explored by these researchers), are believed to have much greater mobility. However, far less is known about these exotic materials or their cheap mass production; thus, they require more comprehensive modeling.

Working with experimentalists at MIT, Klimeck and Luisier reproduced the characteristics of the group’s novel transistors, which use indium-gallium arsenide, a material that has long enticed researchers because of its high electron mobility.

“People have said that gallium-arsenide is the material of the future, and that it always will be,” joked Klimeck.

The validation of the OMEN tool gives researchers the confidence to design more efficient transistors with different materials, predict the effects of size on performance, or even model the effects of impurities on the flow of atoms.

“How big should you make one layer? How long should the channel be to get the best

performance?” asked Luisier. “These are some of the technology and design challenges where we can help.”

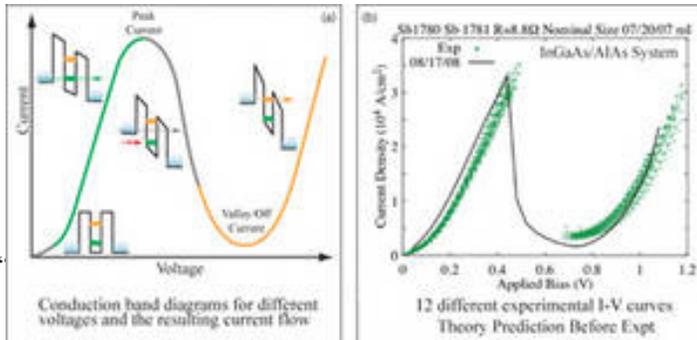
The researchers published several papers explaining their methodology and results, including the lead article in the March/April 2010 issue of *Computing in Science and Engineering*.

At its core, the issue is how to speed electrons through the transistor without hindrance, and with limited vibrational motion, which leads to heat. Over the last year, Luisier has explored this problem, and is working to develop the capability to couple the oscillations of atoms to the motion of the electrons flowing through the transistor material — a process, called electron-phonon scattering, that leads to heat-generation in chips.

“While the physics of this phenomenon was understood in principle, it was deemed an unsolvable problem because it’s computationally intense,” said Klimeck. “Now, with the availability of these big supercomputers, we can run on 70,000 cores for 12 hours, which is the equivalent of 93 years of simulation time on a single CPU, and solve this ‘unsolvable’ problem.”

Representing the interactions between electrons and the surrounding crystal is critical in modeling realistic devices, according to the researchers. Luisier has recently added the phonon scattering component to OMEN.

Meanwhile, researchers under Klimeck are also exploring devices four atoms wide and one atom thick that are predicted to be useful for quantum computing.

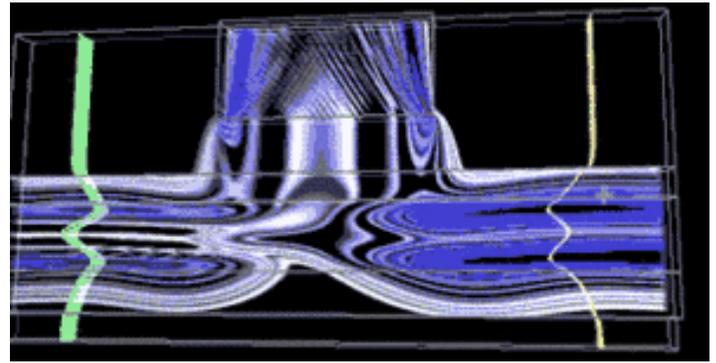


Resonant tunneling diode. (a) A conceptual sketch of a double-barrier structure under various bias conditions, leading to a current turn-on and turn-off with increasing bias. (b) Experimental data from 12 different current and volt (I-V) curves overlapping theoretical predictions of NanoElectronic Modeling 1D (NEMO-1D).

The recent development of the OMEN simulation engine was driven by a Petascale Applications (or "PetaApp") grant from the National Science Foundation, which challenged top HPC users to work together to scale important codes to the petascale and beyond, and to answer questions of pressing social importance.

Klimeck and Luisier’s code has been quite successful at scaling to large numbers of processors. It has proven that it can scale to 220,720 cores on Jaguar at the Oak Ridge National Laboratory with great efficiency.

Though they are now using Department of Energy systems



This physical structure describes a high electron mobility transistor which is intended to carry electrons in the middle of the channel as indicated by horizontal bars. At certain voltage conditions electrons prefer to “tunnel” through to the current regulating gate as demonstrated by the “sand” flowing through the current density field.

for their computing, the scientists say their research would not have progressed as quickly without the presence of the Ranger supercomputer, where they performed simulations for the first two years of the project.

“Ranger completely changed our way of thinking,” Luisier said. “With access to Ranger, I could think about doing these kinds of studies. Before that, it was not possible.”

Developing OMEN’s petascale algorithm is only part of the group’s mission. Based on this work, the scientists have built a suite of tools that can be run interactively on the web by researchers at all levels of experience. Together, these tools make up nanoHUB.org, one of the most advanced community efforts to develop and share tools for simulation.

To date, thousands of researchers have simulated nanoelectronics devices using these tools. Tens of thousands more (including a large pool of students) have learned about nano-simulation through nanoHUB.org, the website created by the Network for Computational Nanotechnology, which Klimeck directs.

As such, the project spreads the message of high-performance computing to a wider audience than ever before, while at the same time extending our capacity to advance technology at a rapid pace.

“These large-scale simulators are critical to continued progress in nanoelectronics,” del Alamo said. “They allow us to predict the performance of transistors years before we can fabricate them in the lab and sort out design options in a way that is far more economical and time efficient than prototyping them all.”

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