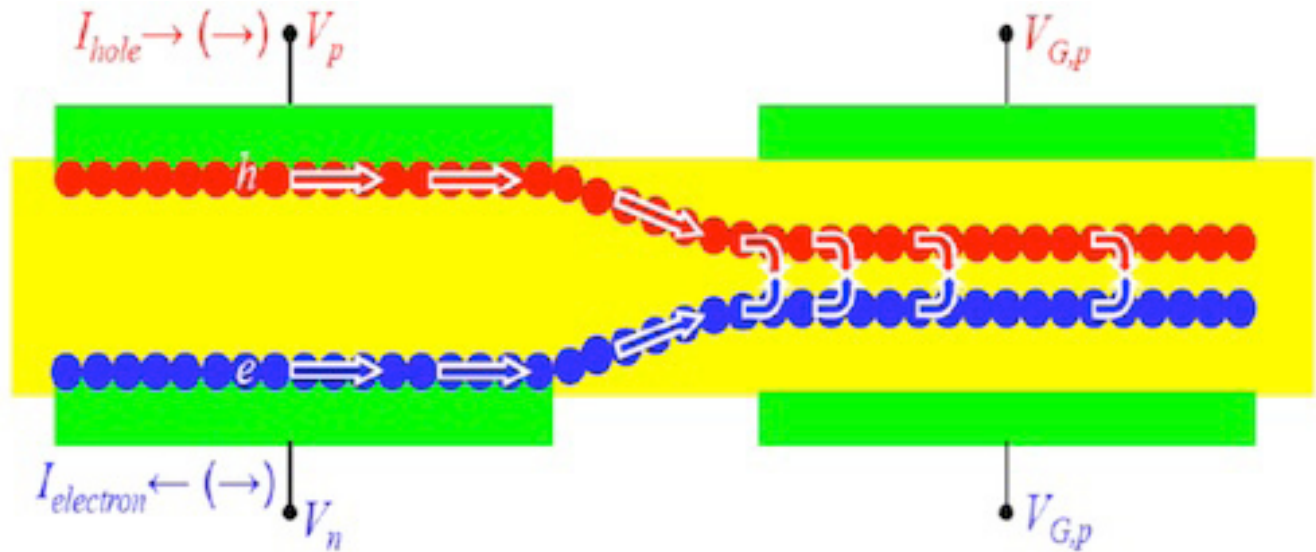


The Frontiers of Future Nanotransistors

Researchers at The University of Texas at Austin simulate graphene transistors for tomorrow's electronic devices



Schematic of the four-terminal BisFET device from the SWAN center at UT-Austin. Two independent graphene layers are connected on the left and right by metal contacts for injection of electron (e) and holes (h) for charge transport. This device has the potential for ultra-low power computing and is one of the devices industry is hoping to launch in 2020, if it can be realized. [Image courtesy: Banerjee et al, Electron device letters, 30, 158 (2009)]

To reach Dr. Bhagawan Sahu's offices at the Microelectronic Research Center in Austin, Texas, one passes glass-faced clean rooms filled with wafer processors and stainless-steel cauldrons. Scientists in white jumpsuits peer through electron microscopes at novel materials, hoping to find ways to improve the electrical characteristics of tomorrow's technologies.

In contrast, Dr. Sahu's office consists of a pair of cubicles behind a heavy door. A few of them together in the hallway make up the offices of the Southwest Academy of Nanoelectronics, or SWAN, a research center exploring next-generation nanotransistors and other future applications.

SWAN is one of four nanoelectronics centers funded through the Nanoelectronics Research Initiative (NRI), a program of the Semiconductor Research Corporation (SRC), the world's leading technology research consortium. SRC is comprised of global semiconductor companies with a vested interest in safeguarding and going beyond Moore's law. The NRI member companies — Texas Instruments, Intel, Global Foundries, IBM and Micron — partner with the National Institute of Standards and Technology and the National Science Foundation to fund research projects throughout the country.

Silicon has long been the workhorse of our digital world, but as

transistors made of the material shrink to the nanoscale, they cease to improve at the same rate. This is due to excessive power consumption in the device and the consequent degradation of its performance.

"The scaling of silicon transistors has driven the economy around the world for the past half century," said Dr. Jeff Welsch, director of the Nanoelectronics Research Initiative at the SRC. "The U.S. is the leader in microelectronics, and to maintain that leadership and to continue to drive the economy, we need to find a way to keep the device scaling going."

One of the solutions being pursued to continue to improve performance is the adoption of new device architectures or new materials. Dr. Sahu, a Research Physicist at The University of Texas at Austin, is part of a nationwide search composed of hundreds of scientists and engineers at universities, research centers, and technology companies. Their goal: to find new nanoscale materials and effects that can be used to replace silicon transistors by the year 2020.

Today's smallest semiconductor transistors are about 32 nanometers (nm) long. Dr. Sahu and the SWAN team aim to make 10nm transistors, with a thickness of less than one nanometer, using graphene. Since it was discovered in the mid-2000s, graphene

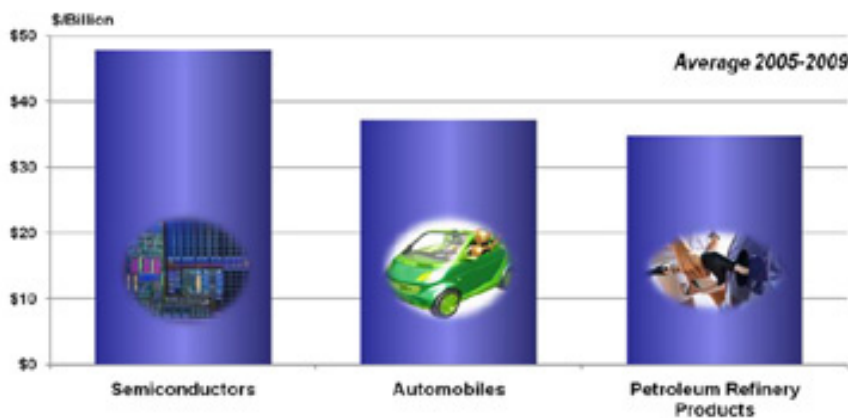
has been lauded as the savior of the semiconductor industry. In 2010, Andre Geim and Konstantin Novoselov, of the University of Manchester, UK, were awarded the Nobel Prize in Physics “for groundbreaking experiments regarding the two-dimensional material.”

Made up of a single layer of graphite, graphene is the thinnest material in the world and possesses electron mobilities (a measure of how fast electrons in a material can move in response to external voltages) higher than silicon. These characteristics are attractive features and have generated tremendous interest from the semiconductor industry. However, as scientists learned more about graphene and proved it could be used as a potential material in transistors, initial excitements gave way to a greater appreciation of the design and fabrication challenges ahead.

After five years of dedicated study, the SWAN center’s novel, graphene-based design was selected by the SRC as one of only a few device ideas to be studied further. Each of these design possibilities provides a different challenge at the atomic level.

“Understanding the device components atomistically through simulations has become inevitable in these nanoscale devices,” Dr. Sahu said. “Our efforts at SWAN provide the community with the simulation results, which are obtained by virtual experiments before any real experiments are performed.”

Semiconductors Have Been America’s Largest Export Over the Last Five Years



Source: U.S. International Trade Commission.

The initial philosophy of the NRI was to “let a thousand flowers bloom,” funding researchers to explore many ideas, including different devices based on graphene and other novel materials. But as the timeline for launching a new processor approaches, the research competition is shifting into overdrive. In January 2011, the project moved into “Phase 1.5”.

“We asked each of the centers to take the devices they thought were most promising and focus all of their efforts on those,” said Dr. Welser.

SWAN selected a graphene-based collective charge system. The device structure, which they call the bilayer pseudospinronic field-effect transistor (or BiSFET), is based on two layers of graphene separated by a super-thin insulator or air or a vacuum [see figure, above]. In the device, pseudospin refers to the presence of charge either on the top layer or the bottom layer, much like electron “spin” in quantum mechanics, which can take two possible values.

The physics of the device is based on collective charge motion, which forms a superfluid state at room temperature under certain conditions.



Dr. Bhagawan Sahu, research scientist at the Southwest Academy of Nanoelectronics (SWAN).

“In this structure, all of the electrons want to be in one layer or the other,” Dr. Welser explained. “By applying a very small voltage — on the order of 25 millivolts — you can get all of the charge to jump from one side to the other. It acts like a switch, which is exactly how we want our transistors to act.”

Prof. Allan MacDonald at The University of Texas at Austin proposed the theory behind the BisFET device, and Prof. Sanjay K. Banerjee (the director of the SWAN center), Prof. Leonard F. Register, and Dr. Emanuel Tutuc, also from UT-Austin, explored the device design and metrics in depth. The simulations necessary to understand the formation of the superfluid phase in graphene bilayers are now carried out by Prof. Register’s group.

Dr. Sahu’s simulations have been crucial to understanding the internal and external variables that can affect the device performance.

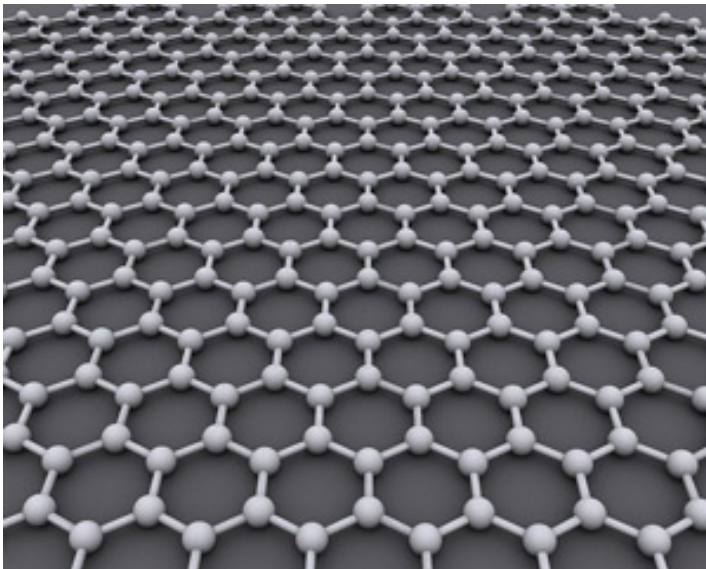
“Atomistic simulations are necessary to understand the nanoscale effects arising from metal-graphene and metal-dielectric contacts,” Dr. Sahu Said.

The collective motion of the charge carriers in BisFET devices have an advantage over current silicon systems: more charges can be collected using less voltage, increasing

the performance and decreasing the overall power consumption of the device. If the SWAN researchers can overcome the challenges involved in fabricating and demonstrating the BisFET devices, this particular transistor may be the game changer that the semiconductor industry is betting on.

The Next Phase of Discovery

In 2013, the SRC hopes that one or two nanotransistor designs will emerge as promising enough to justify expanded work on proof-of-concept demonstrations. This will require extensive research, initially in the university centers and eventually in industry labs. Even if all goes well, it will be challenging to introduce these devices into products by 2020, since it often takes 10 years or more from initial discovery to commercial implementation for new technology.



Graphene is an atomic-scale honeycomb lattice made of carbon atoms.

If the devices use very different materials or structures, this will be no small endeavor. To convert fabrication facilities from silicon to graphene, for example, is expected to cost billions of US dollars. That is, if it is even possible to produce graphene in large enough quantities to realize carbon age electronics. (There are efforts by another SWAN member, Prof. Rodney S. Ruoff of The University of Texas at Austin, working with Texas Instruments' SWAN assignee, Dr. Luigi Colomboto, to grow large area graphene films on metal substrates by chemical vapor deposition, which is critical for the success of the center's BisFET device.)

Over the course of the last four years, Dr. Sahu has developed much of the underlying knowledge of graphene behavior at the nanoscale through numerical simulations on the Ranger supercomputer at the Texas Advanced Computing Center (TACC).

Using one of the largest, most advanced supercomputers available to the scientific community has allowed Dr. Sahu to investigate single-layer, bilayer, and multilayer forms of graphene. It has also let him experiment, virtually, with different widths, lengths, layer orientations, layer stackings and external voltages for graphene

ribbons and flakes, to see how these variables influence the electronic properties including the electron band gap, magnetism and other related factors.

“The simulations are playing a major role in elucidating the interplay of the structure and the electronic properties of graphene,” Dr. Sahu said. “We’re building component by component, so we have an integrated view of what each part does and how it affects the whole device.”

The flurry of research into graphene has led to other niche applications that may have equally wide-reaching effects. Graphene is believed to be a potential material for memory systems, and for clean energy technology such as lithium-ion battery and solar photovoltaic cells. The common denominator in all of these applications is a need for smaller, faster, more energy efficient devices that make use of novel materials.

“Energy is one of the pressing problems for the society, and a lot of energy is consumed in present digital devices,” said Dr. Sahu. “If we can design a device that uses a billion times less power than a silicon transistor, as BisFET seems to promise, we can build on that kind of technology for the next few generations after 2020.”

May 18, 2011